What is Claimed is:

1. A semiconductor memory, comprising:

a plurality of memory cells, the memory cells being connected to first lines and to second lines, the second lines crossing the first lines, each memory cell having storage capacitor and a selection transistor, the memory cells form at least one memory cell array, wherein the first lines run divergently with respect to one another, the second lines are curved, a memory cell is connected at each crossing point between a first line and a second line, each of the first lines having memory cells connected thereon, the respective storage capacitor being laterally offset alternately on each side of the respective first line.

2. The semiconductor memory as claimed in claim 1, wherein the first lines extend divergently from a logic area to the memory cells in at least one memory cell array.

3. The semiconductor memory as claimed in claim 1, wherein the memory cells form at least one memory cell array, at the memory cell array having the form of an annular portion, the first lines diverging radially, and the second lines curving arcuately.

4. The semiconductor memory as claimed in claim 1, wherein one or more memory cell arrays surround a logic area annularly.

5. The semiconductor memory as claimed in claim 1, wherein the first lines are bit lines and the second lines are word lines.

6. The semiconductor memory as claimed in claim 1, wherein the first lines are word lines and the second lines are bit lines.

7. The semiconductor memory as claimed in claim 1, wherein two memory cells are connected to two mutually adjacent bit lines, the two memory cells being connected to the same word line, the two memory cells having respective storage capacitors adjacent to one another along the same word line, the two memory cells being connected to two mutually adjacent bit lines.

8. The semiconductor memory as claimed in claim 1, wherein the storage capacitors are trench capacitors buried in a semiconductor substrate.

9. The semiconductor memory as claimed in claim 8, wherein at least one further logic area is provided on the semiconductor substrate and is arranged between a memory area and an edge of the semiconductor substrate the further logic area not surrounded by memory areas.

10. The semiconductor memory as claimed in claim 1, wherein the selection transistors are vertical field effect transistors whose gate electrodes are connected to the word lines.

11. The semiconductor memory as claimed in claim 10, wherein at least one further logic area is provided on the semiconductor substrate and is arranged between a memory area

and an edge of the semiconductor substrate the further logic area not surrounded by memory areas.

12. The semiconductor memory as claimed in claim 1, wherein the semiconductor memory is a dynamic read/write memory.

13. A semiconductor memory, comprising:

a plurality of memory cells, the memory cells being connected to first lines and to second lines, the second lines crossing the first lines, each memory cell having a storage capacitor and a selection transistor, the memory cells forming at least one memory cell array,

wherein the first lines run divergently with respect to one another, the second lines are curved, a memory cell is connected at each crossing point between a first line and a second line, each of the second lines having memory cells being connected thereon, the respective storage capacitor being laterally offset alternately on each side of the respective second line.

14. The semiconductor memory as claimed in claim 13, wherein the first lines extend divergently from a logic area to the memory cells in at least one memory cell array.

15. The semiconductor memory as claimed in claim 13, wherein the memory cells form at least one memory cell array, the memory cell array having the form of an annular portion, the first lines diverging radially, and the second lines curving arcuately.

16. The semiconductor memory as claimed in claim 13, wherein one or more memory cell arrays surround a logic area annularly.

17. The semiconductor memory as claimed in claim 13, wherein the first lines are bit lines and the second lines are word lines.

18. The semiconductor memory as claimed in claim 13, wherein the first lines are word lines and the second lines are bit lines.

19. The semiconductor memory as claimed in claim 13, wherein two memory cells are connected to two mutually adjacent bit lines, the two memory cells being connected to the same word line, the two memory cells having respective storage capacitors adjacent to one another along the same word line, the two memory cells being connected to two mutually adjacent bit lines.

20. The semiconductor memory as claimed in claim 13, wherein the storage capacitors are trench capacitors buried in a semiconductor substrate.

21. The semiconductor memory as claimed in claim 20, wherein at least one further logic area is provided on the semiconductor substrate and is arranged between a memory area and an edge of the semiconductor substrate the further logic area not being surrounded by memory areas.

22. The semiconductor memory as claimed in claim 13, wherein the selection transistors are vertical field effect transistors whose gate electrodes are connected to the word lines.

23. The semiconductor memory as claimed in claim 22, wherein at least one further logic area is provided on the semiconductor substrate and is arranged between a memory area and an edge of the semiconductor substrate the further logic area not being surrounded by memory areas.

24. The semiconductor memory as claimed in claim 12, wherein the semiconductor memory is a dynamic read/write memory.